ABSTRACT OF THE DISCLOSURE

A processor (e.g., a co-processor) executes a stack-based instruction set and another instruction in a way that accelerates the execution of the stack-based instruction set, although code acceleration is not required under the scope of this disclosure. In accordance with at least some embodiments of the invention, the processor may comprise a multi-entry stack usable in at least a stack-based instruction set, logic coupled to and managing the stack, and a plurality of registers coupled to the logic and addressable through a second instruction set that provides register-based and memory-based operations.